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Thriving in the world of high-speed serial interconnects

July 16, 2003

presented by:

Art Porter

Agenda

- Introduction
- Design stage
- Electrical faults
- Statistics
- PCI Express example
- Real-life examples
- Tools for success

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Goals

- Meet objectives for performance and reliability
- Finish your project on time and in budget

In the new world of high-speed serial interconnects

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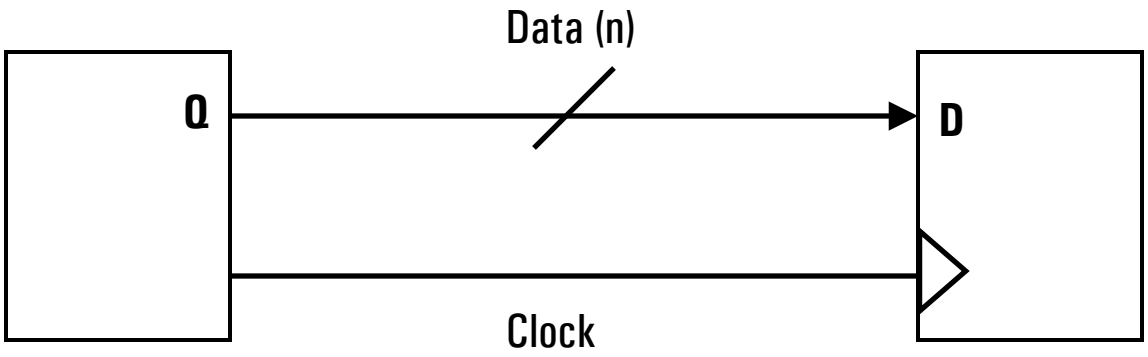
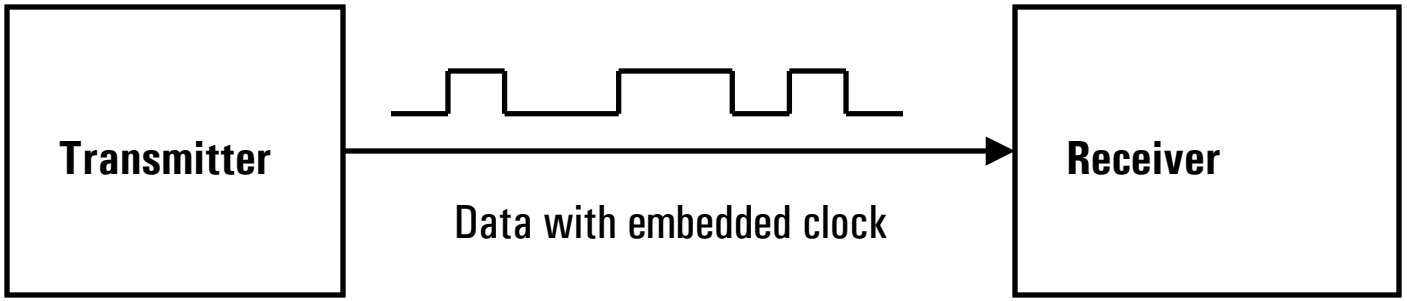
Serial Data With Embedded Clock



The old way



The new way

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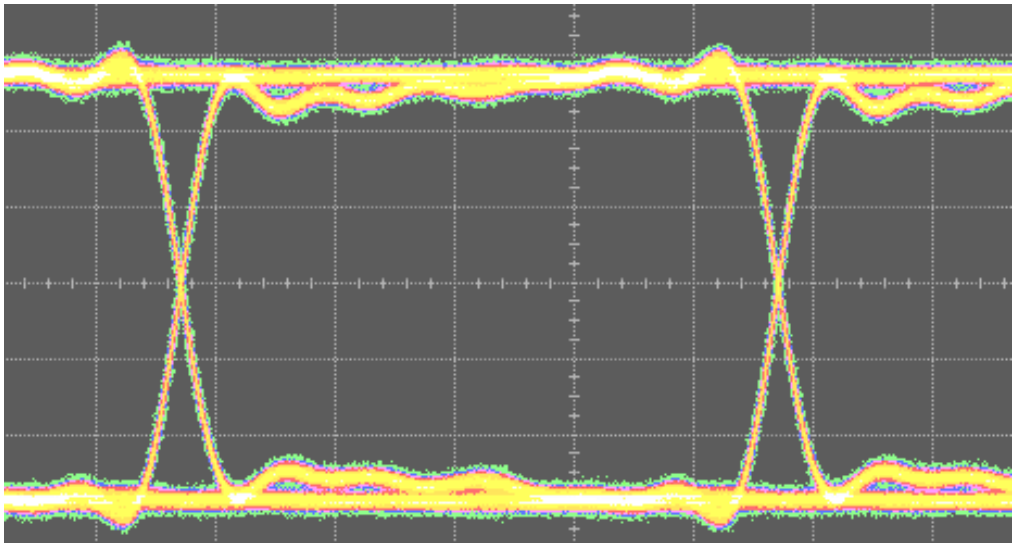
Abstractions

- Physical layer (signal integrity)
- Protocol
- Data transfer



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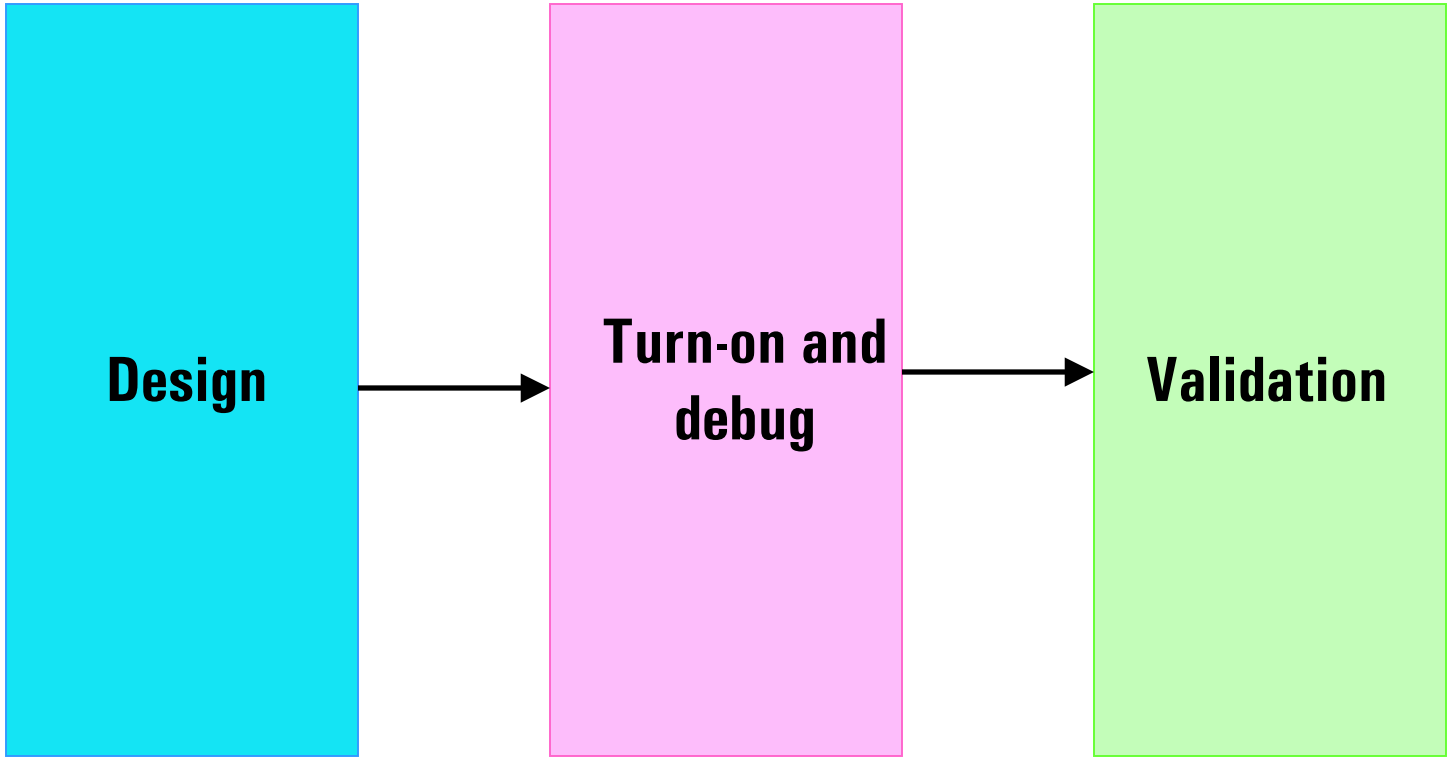
Critical Skills and Tools Required

- Circuit design and analysis
  - Lumped parameters (R/L/C)
  - Transmission lines (s-parameters)
- Statistics
- Measurement

Process



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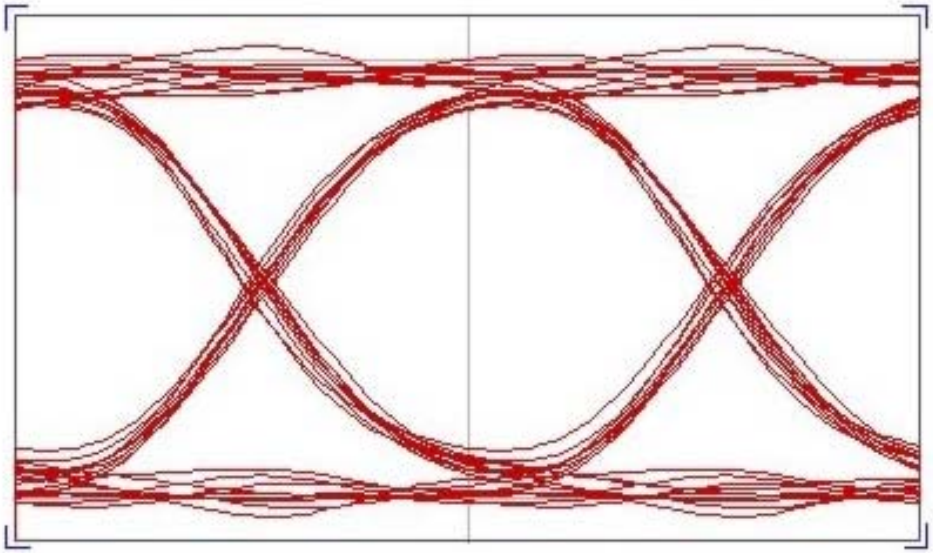
Design

- The circuit now includes everything
  - PC board traces
  - Vias
  - Pins
  - Connectors
  - Bond wires
  - Metallization

Models

- Good designs start with good models
- Good models start with good measurements

Simulated eye diagram from an Agilent Physical Layer Test System



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Models – What's In a Model?

- Every R has some C and L
- Every C has some L
- If the manufacturer won't or can't give you accurate models, you may have to create them.

What you thought you had

Models – What's In a Model?

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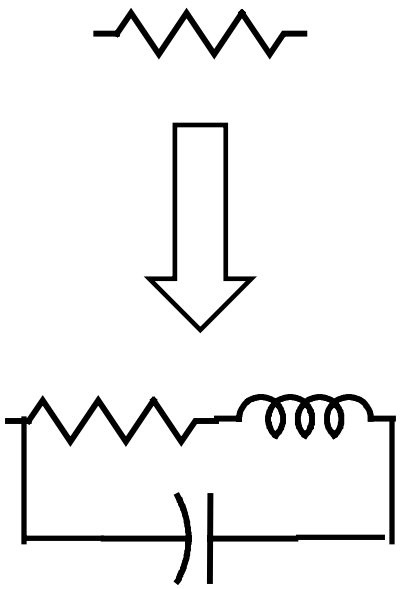

What you really have

Models – Which To Use?

- Don’t assume model parameters published by trade associations
- Allow for multiple vendors, process changes by simulating with worst-case models
- For transmission lines, decide if you need
  - Single-element
  - Multi-section, lumped-parameter
  - Full transmission line

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Types Of Faults

- Single-net faults
- Multiple-net faults (crosstalk)
- Power and ground faults

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Single-Net Faults

- Reflections
- Over or under-damping
- Loss
- Dispersion

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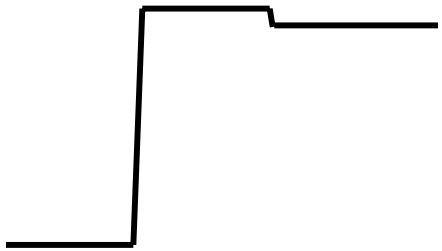
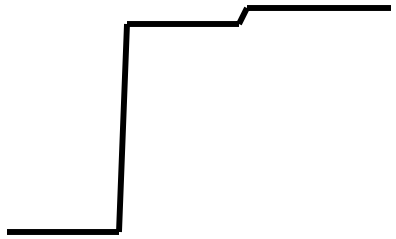
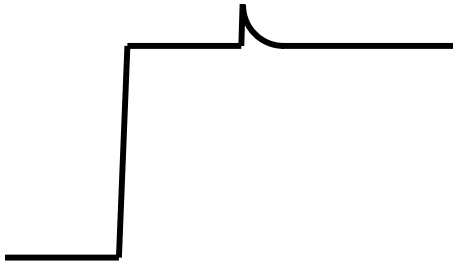
Reflections



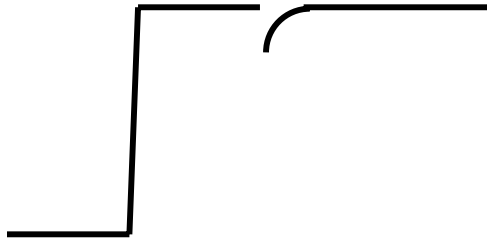
Zterm < Z0



Zterm > Z0



Inductive discontinuity



Capacitive discontinuity

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Avoiding Reflections

- Start with good models
- Validate models
- Validate structure using TDR or VNA
- Hint: Use the driver and your scope as a TDR

Fun With Frequency

0101010101010101

0011001100110011

0000111100001111

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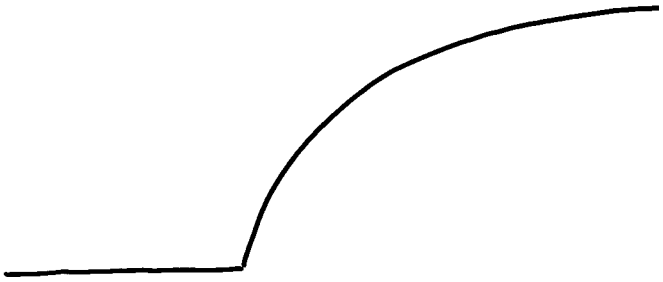
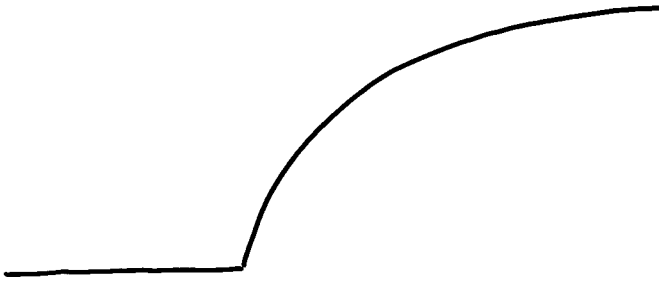
Intersymbol Interference (ISI)



Single-pole RC time constant

Intersymbol Interference (ISI)



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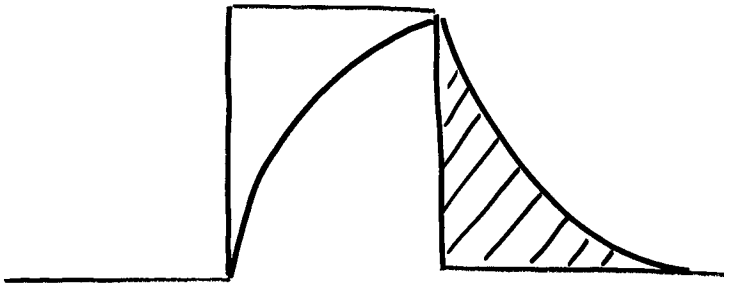
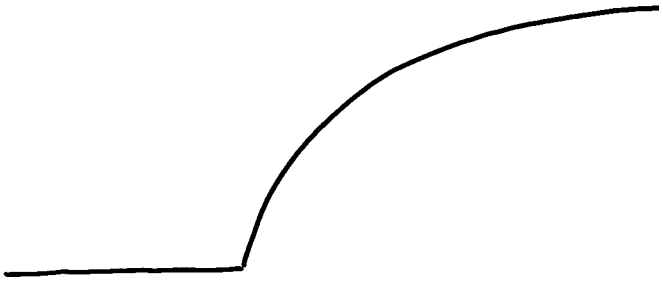


Effect on an isolated “1”

Intersymbol Interference (ISI)



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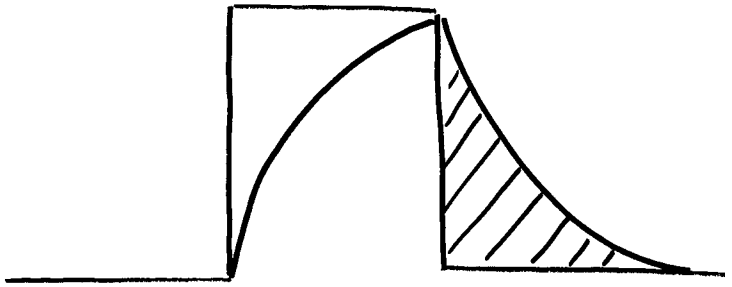

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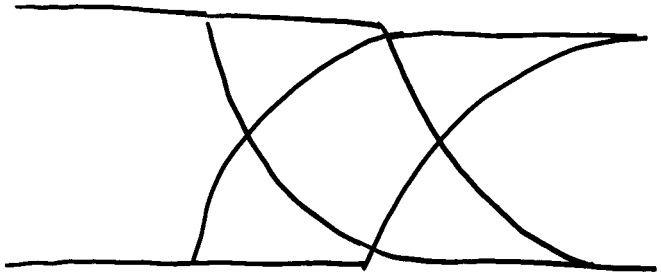

Effect on data eye

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Likely Causes Of ISI

- Over or underdamping
- Dispersion
- Reflections

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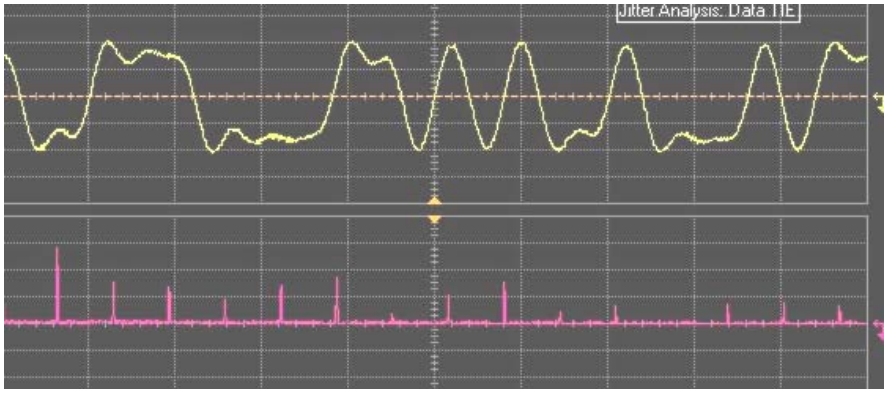
ISI Diagnostic Clues

In a PRBS sequence (pseudorandom binary sequence), ISI will exhibit energy peaks in the jitter spectrum at multiples of F/2(sequence length), where F = bit rate.

If possible, try varying PRBS sequence lengths and watch for changes in the jitter spectrum.



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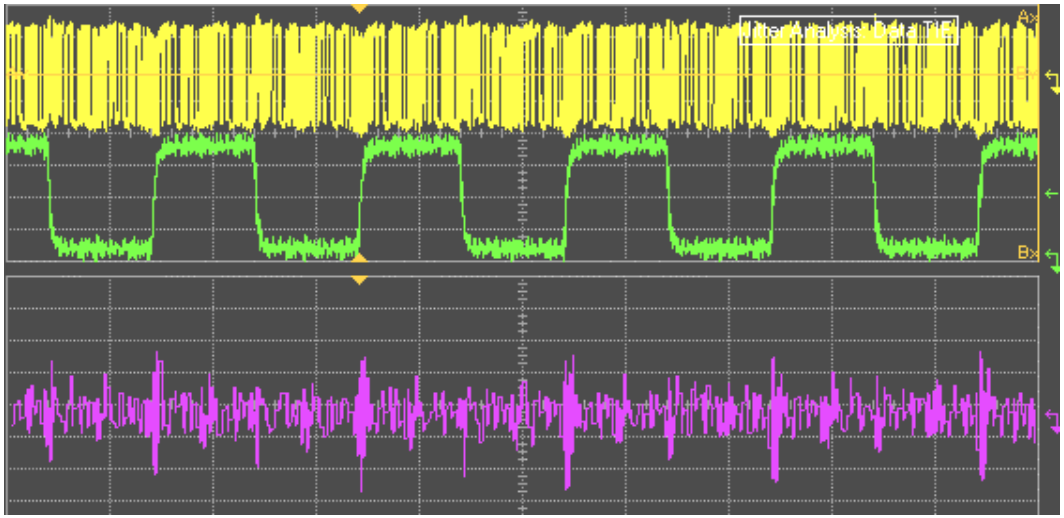
Multiple-Net Faults - Crosstalk

- Can be difficult to distinguish from power and ground coupling phenomena
- Often gets translated into jitter

Crosstalk Sleuthing

- Should show up in the spectrum
- Histogram will be non-Gaussian
- Try triggering on suspected source



Yellow: signal with jitter

Green: Offending source of jitter

Purple: Jitter trend

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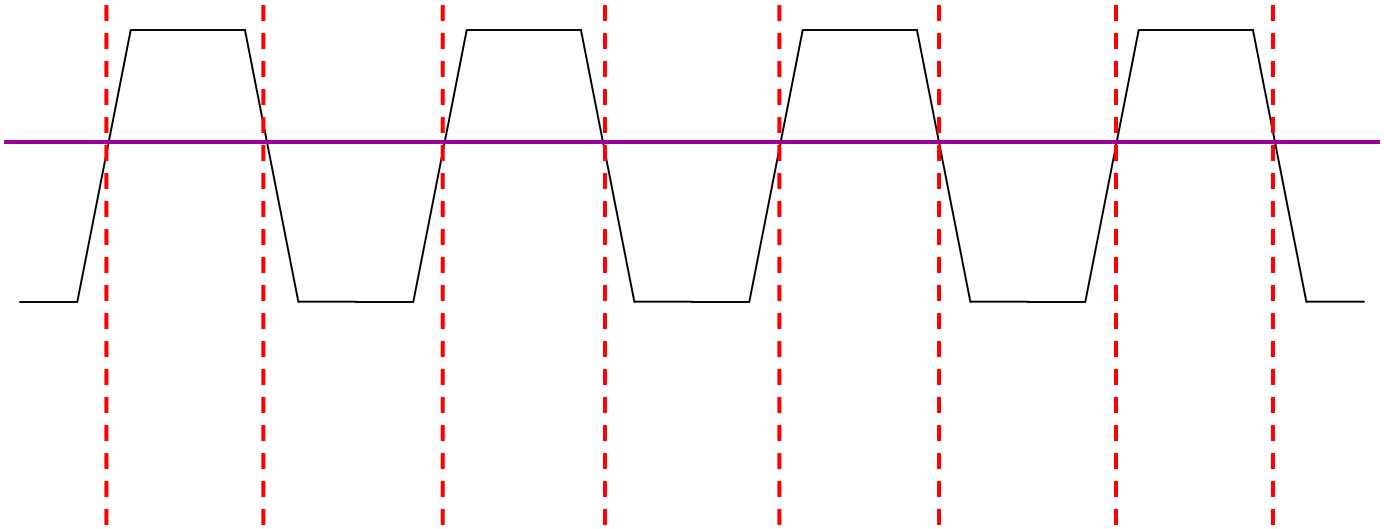
Power And Ground

- Sometimes difficult to distinguish from crosstalk
- Indicator: Affects many or all nodes
- Power and ground faults can impact output delays, thus adding jitter

Translating Noise To Jitter



Constant threshold at the proper level

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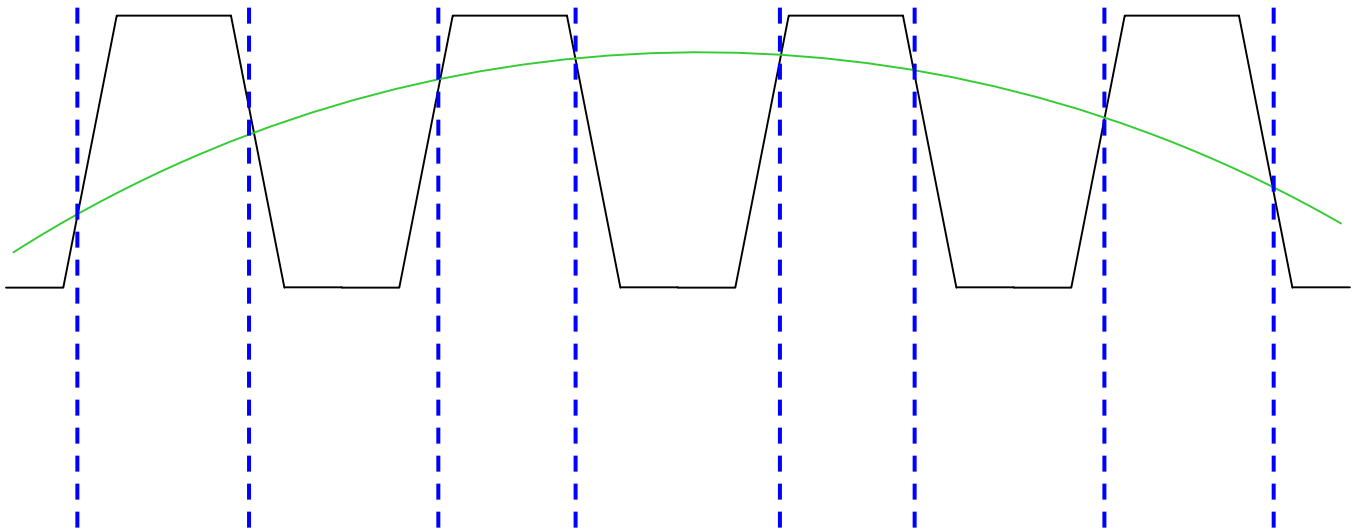
Translating Noise To Jitter



Varying threshold

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Statistics

The question is not: Did it pass?

The questions are:

- What is the failure rate?
- How much margin do I have?

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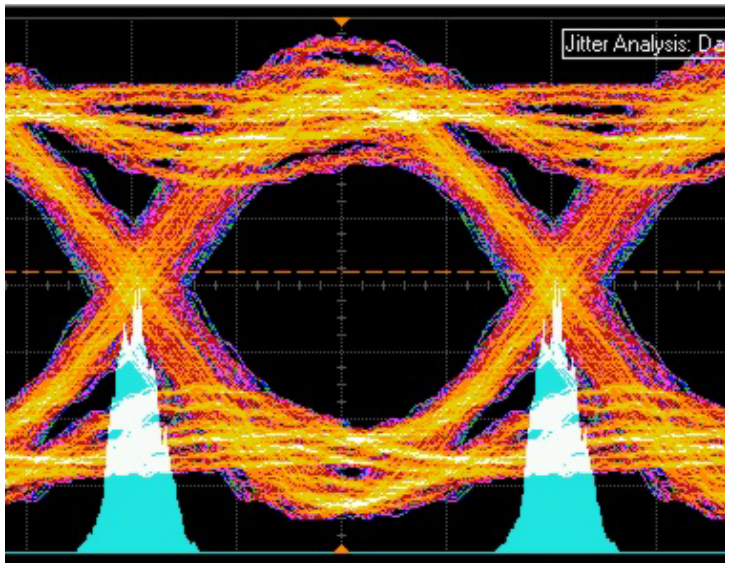
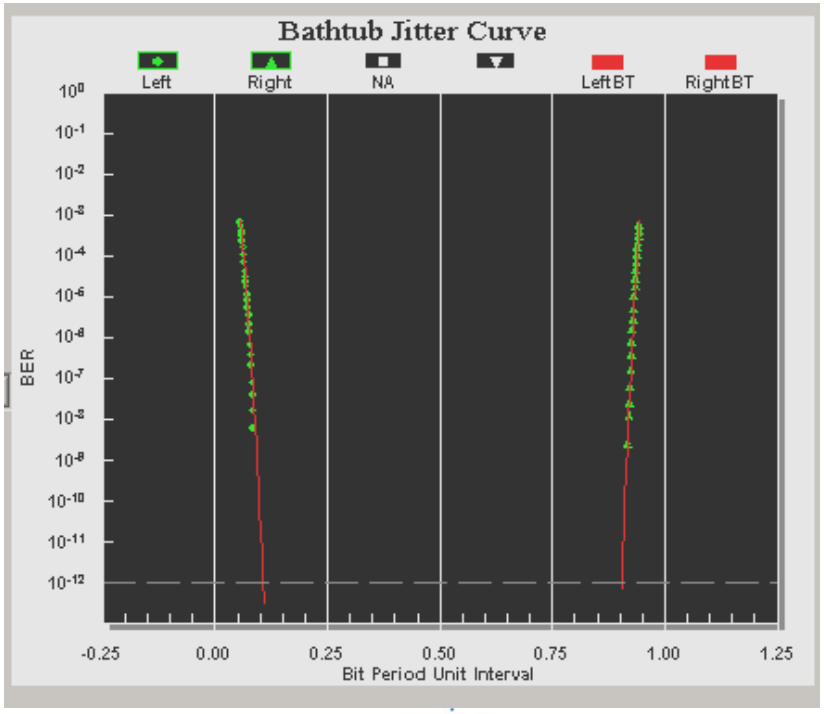
Statistics

- Determine target BER
- Decide on an acceptable confidence interval





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PCI Express Measurement Example

- Need to recover clock from the data stream
- PCI Express is differential

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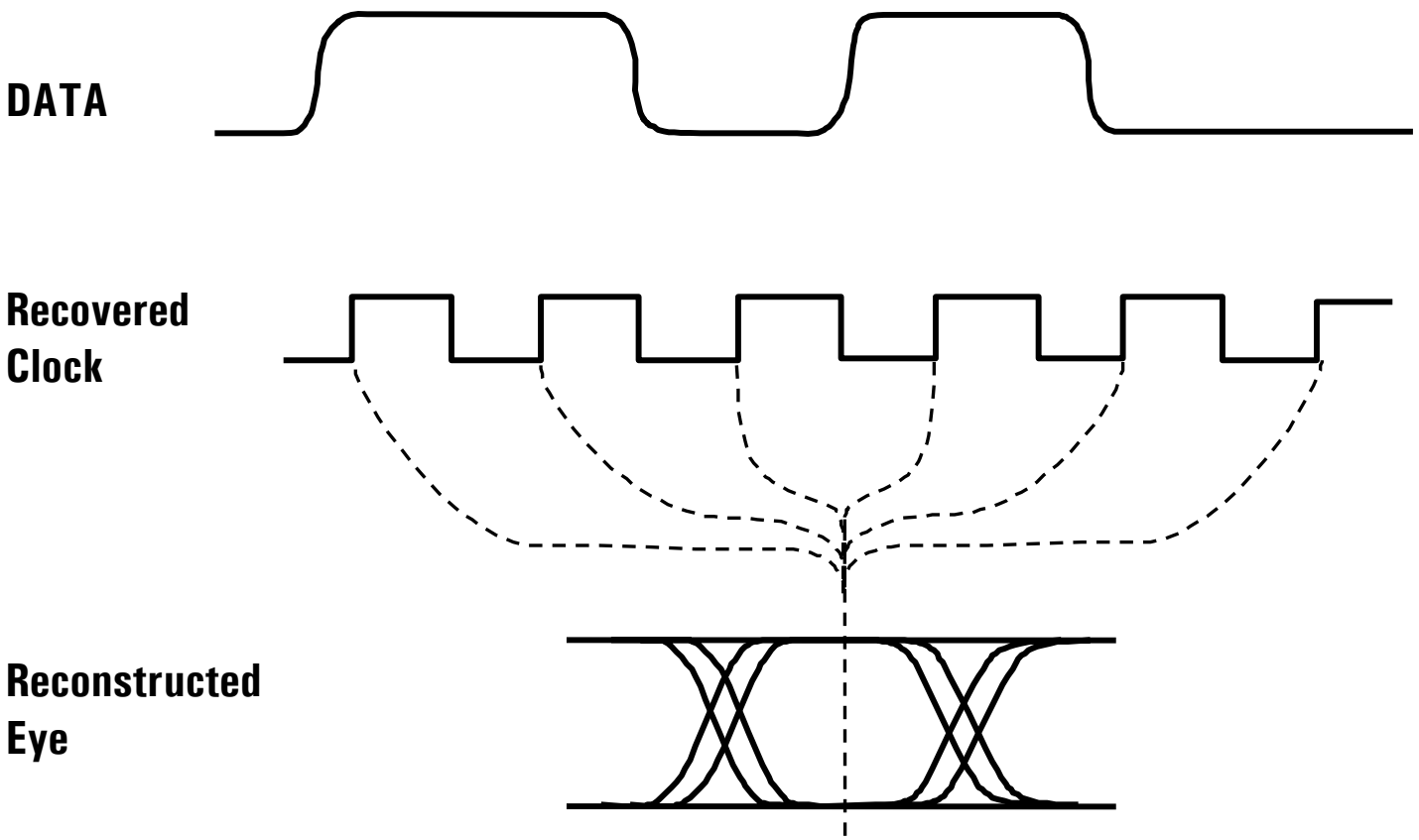
Reconstructing the Eye



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PCI Express Showing Clock

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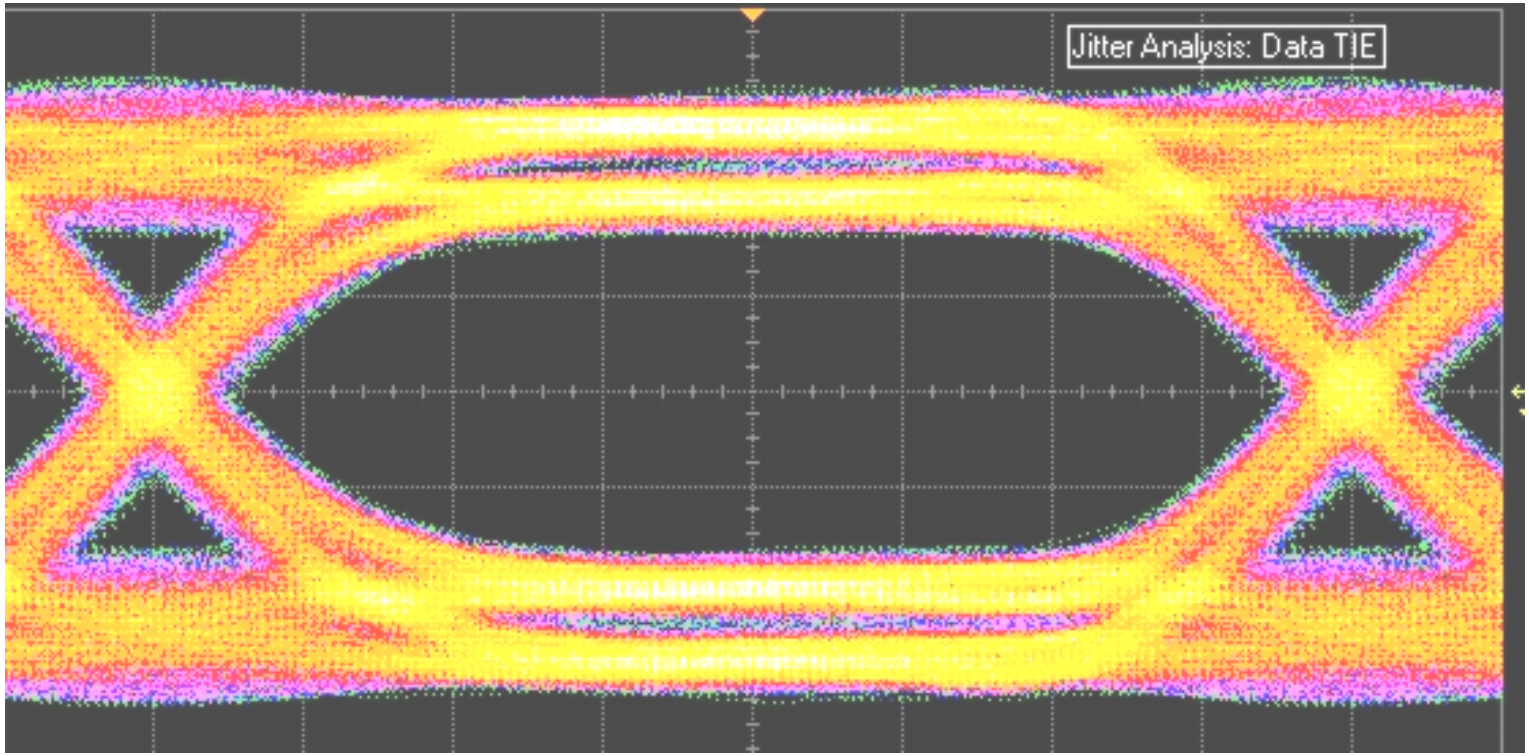
PCI Express Eye, Color Graded



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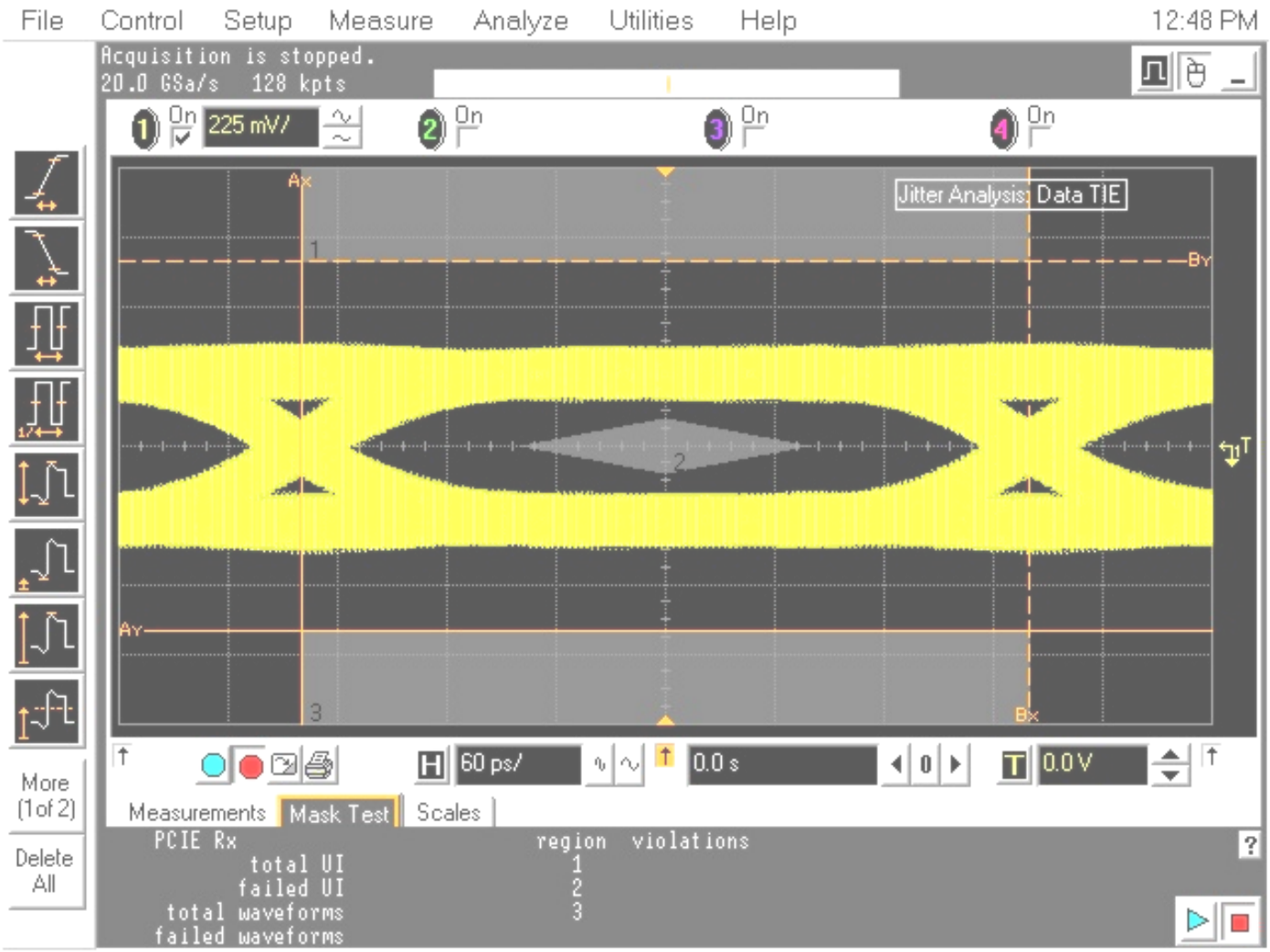
PCI Express Eye With Mask



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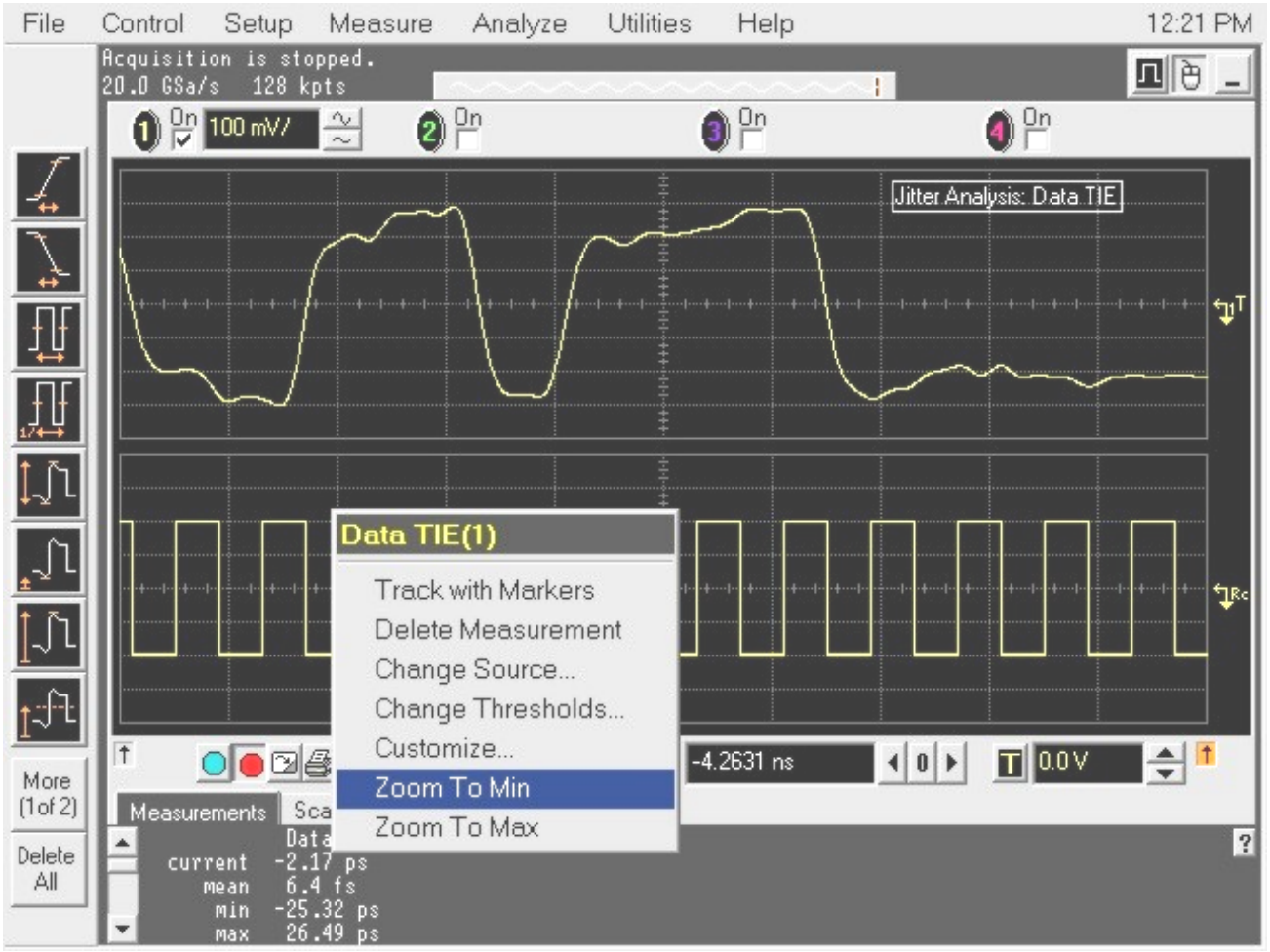
PCI Express, Finding Worst Cases



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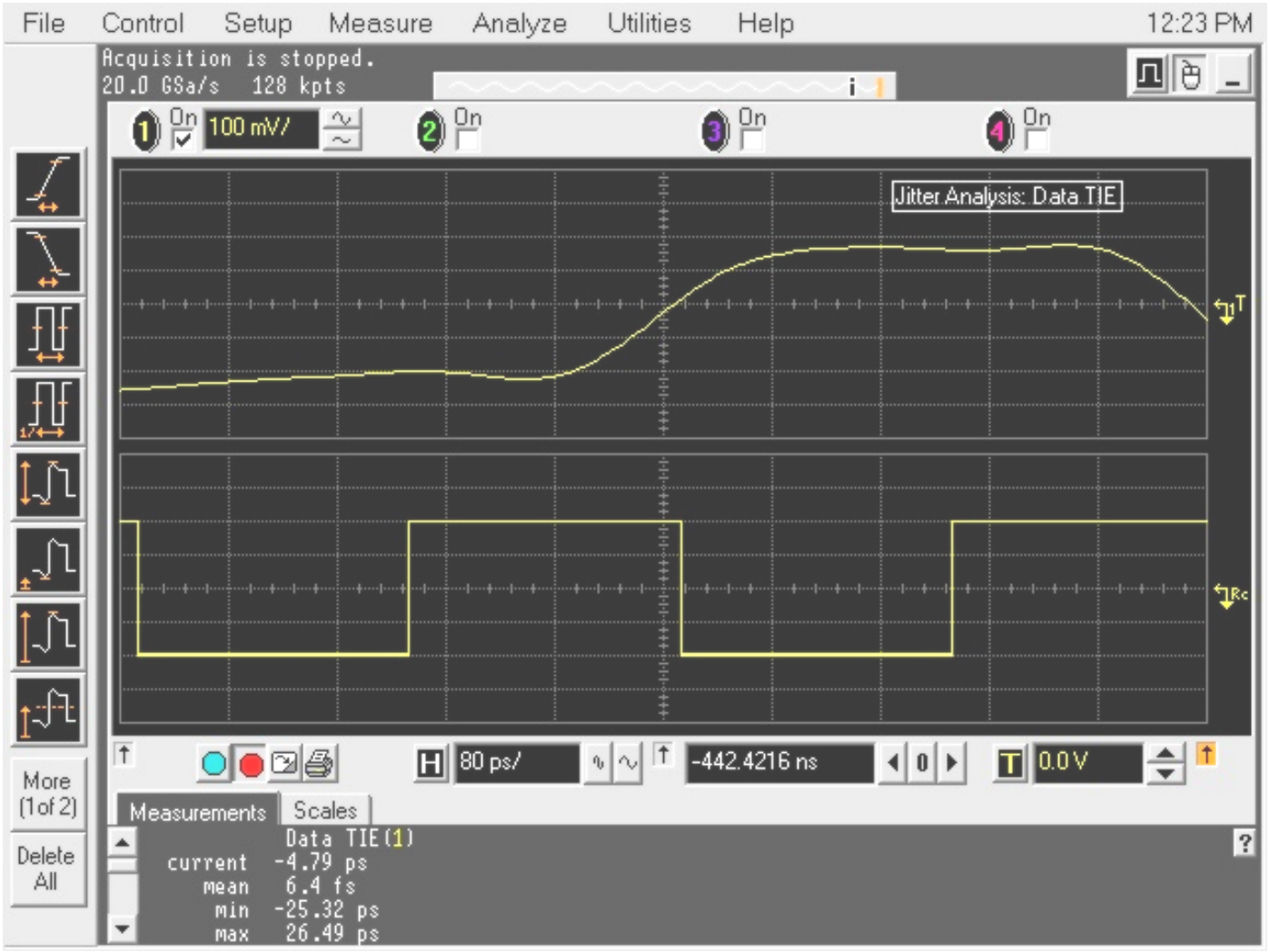
PCI Express, Finding Worst Cases



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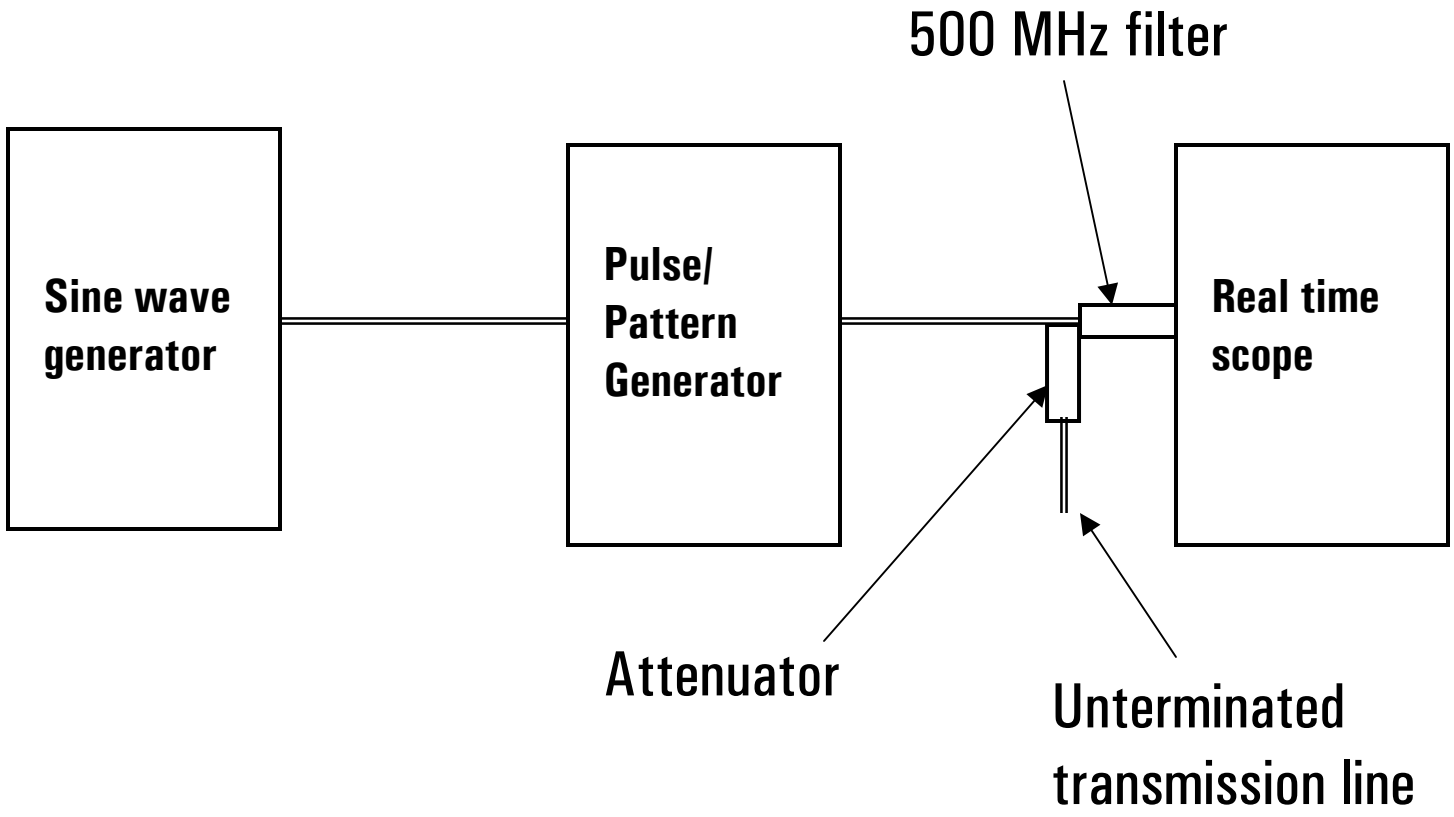
Real life examples

- ISI
  - Band-limiting
  - Reflections
- Deterministic, periodic jitter
- Random jitter
- All of the above
- Duty cycle distortion

Setup For Examples



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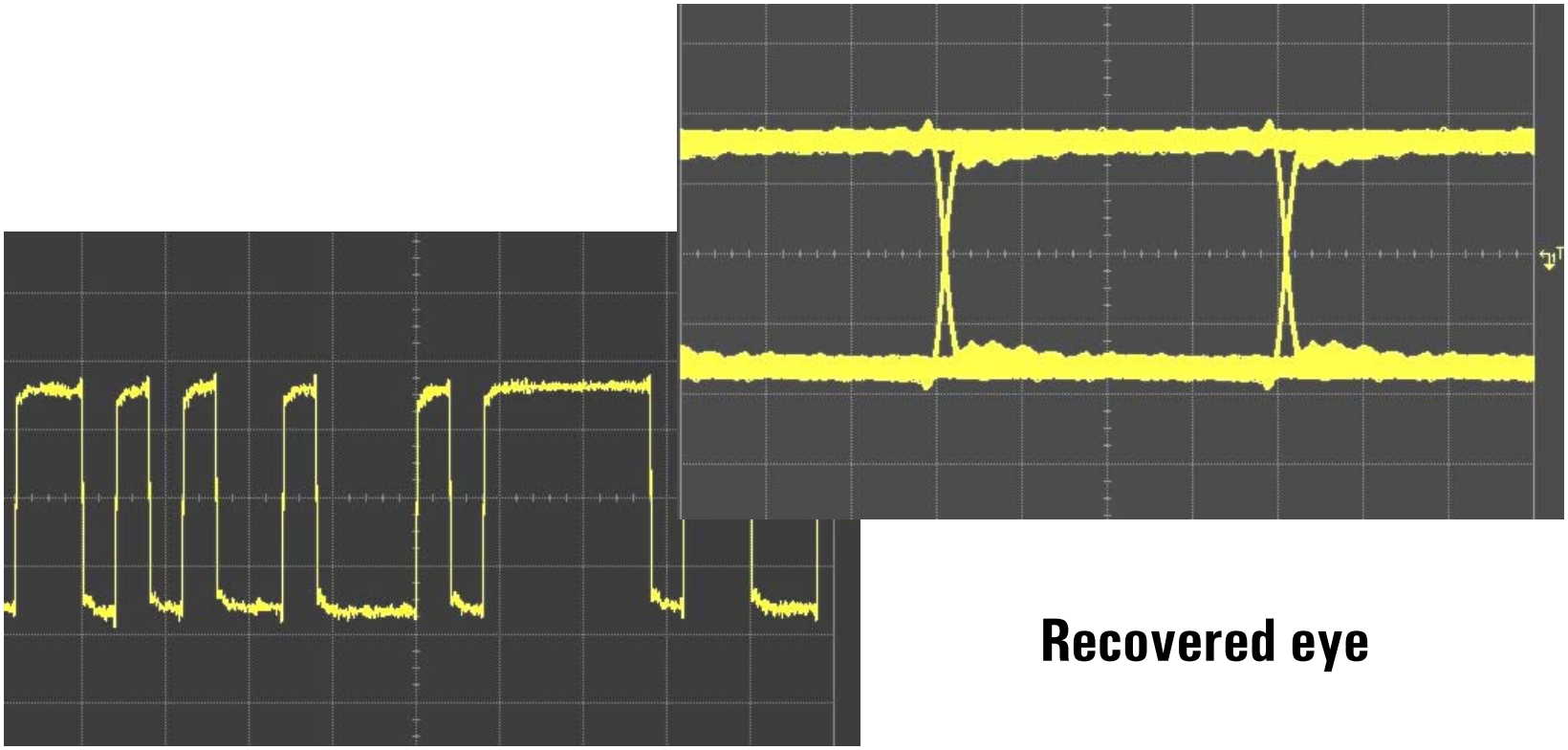
Reference: 500 Mb/s



Recovered eye

Data stream

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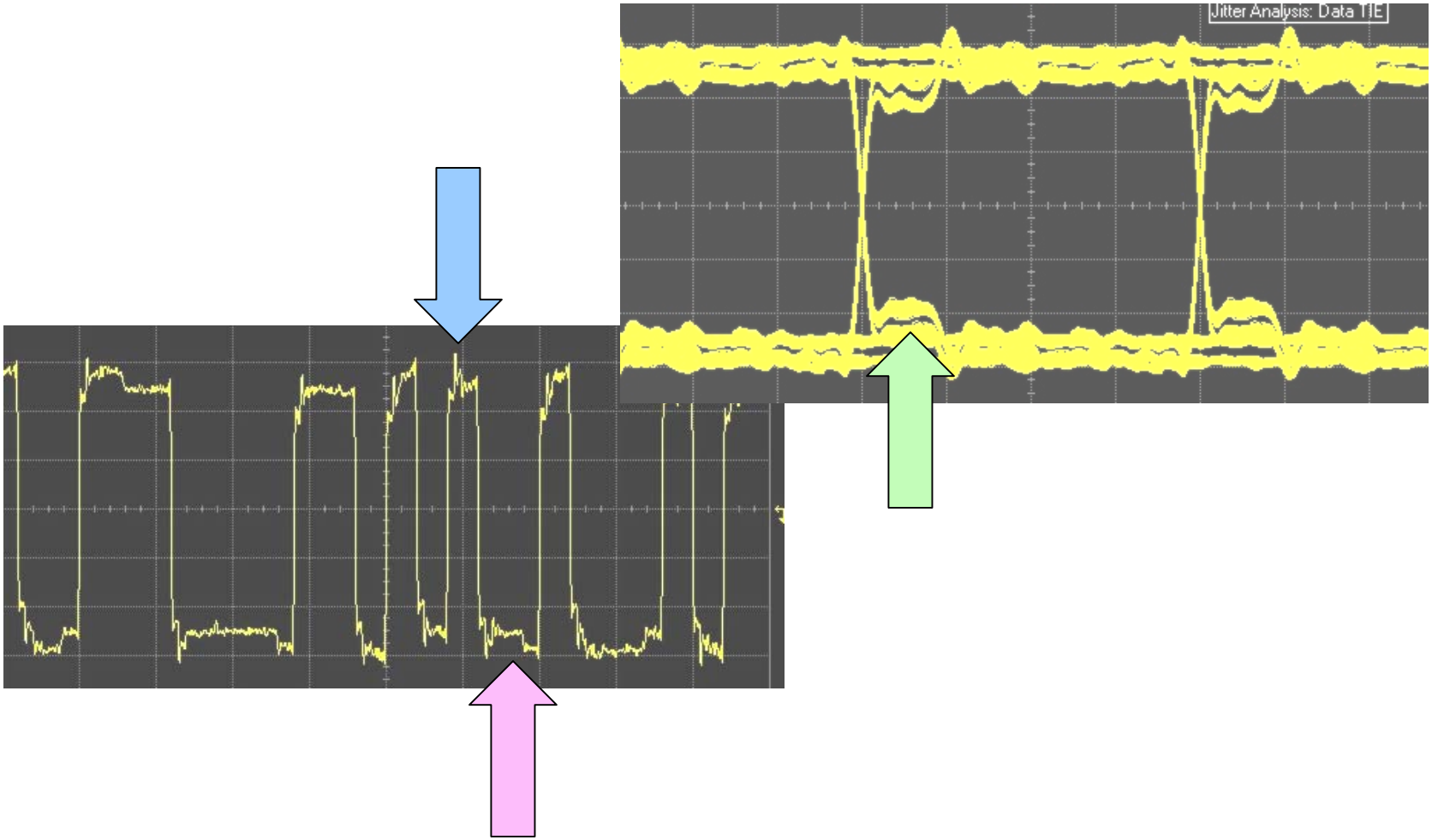
Reflection



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Reflection – Jitter Spectrum

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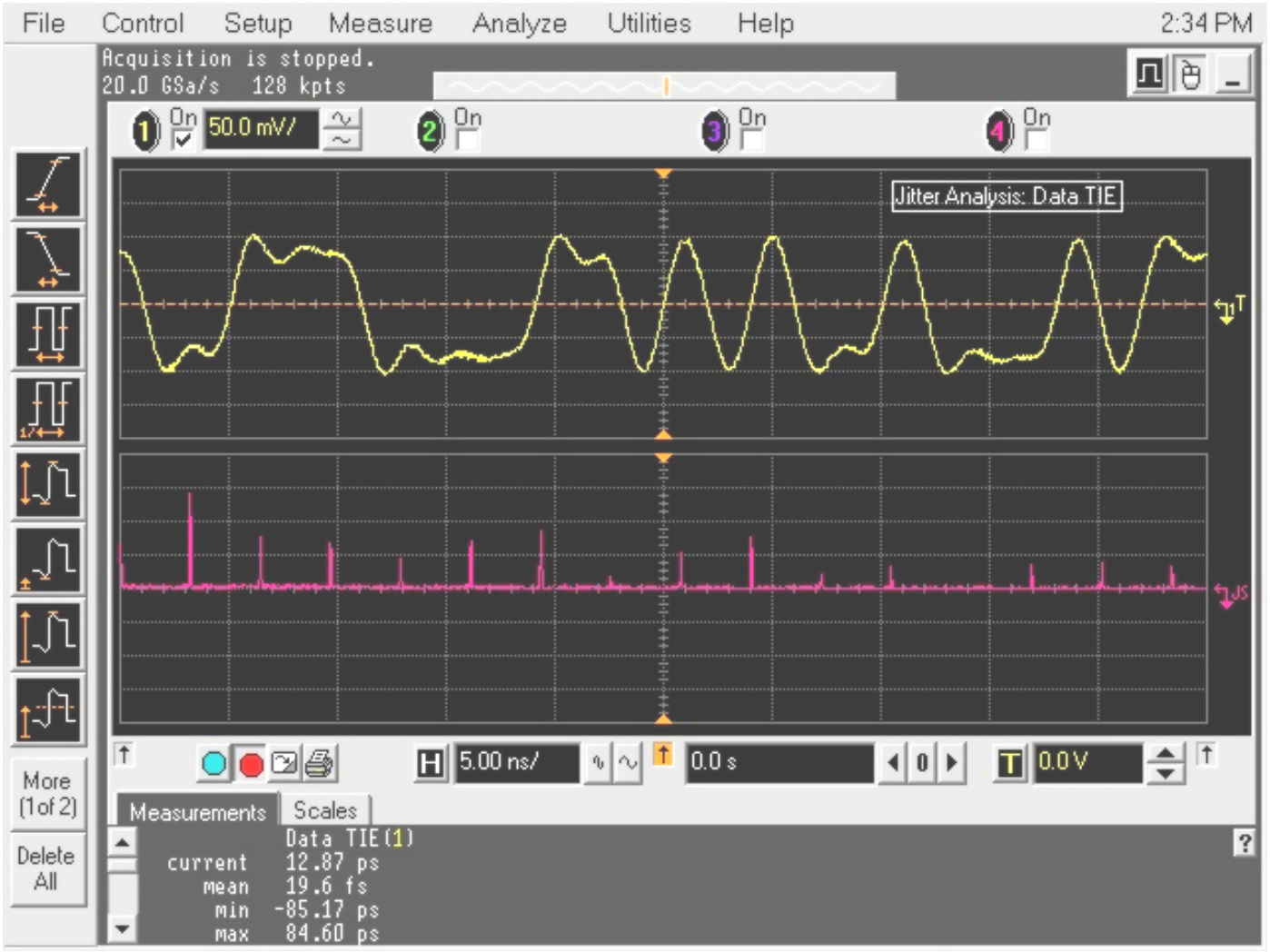
Bandwidth Limiting



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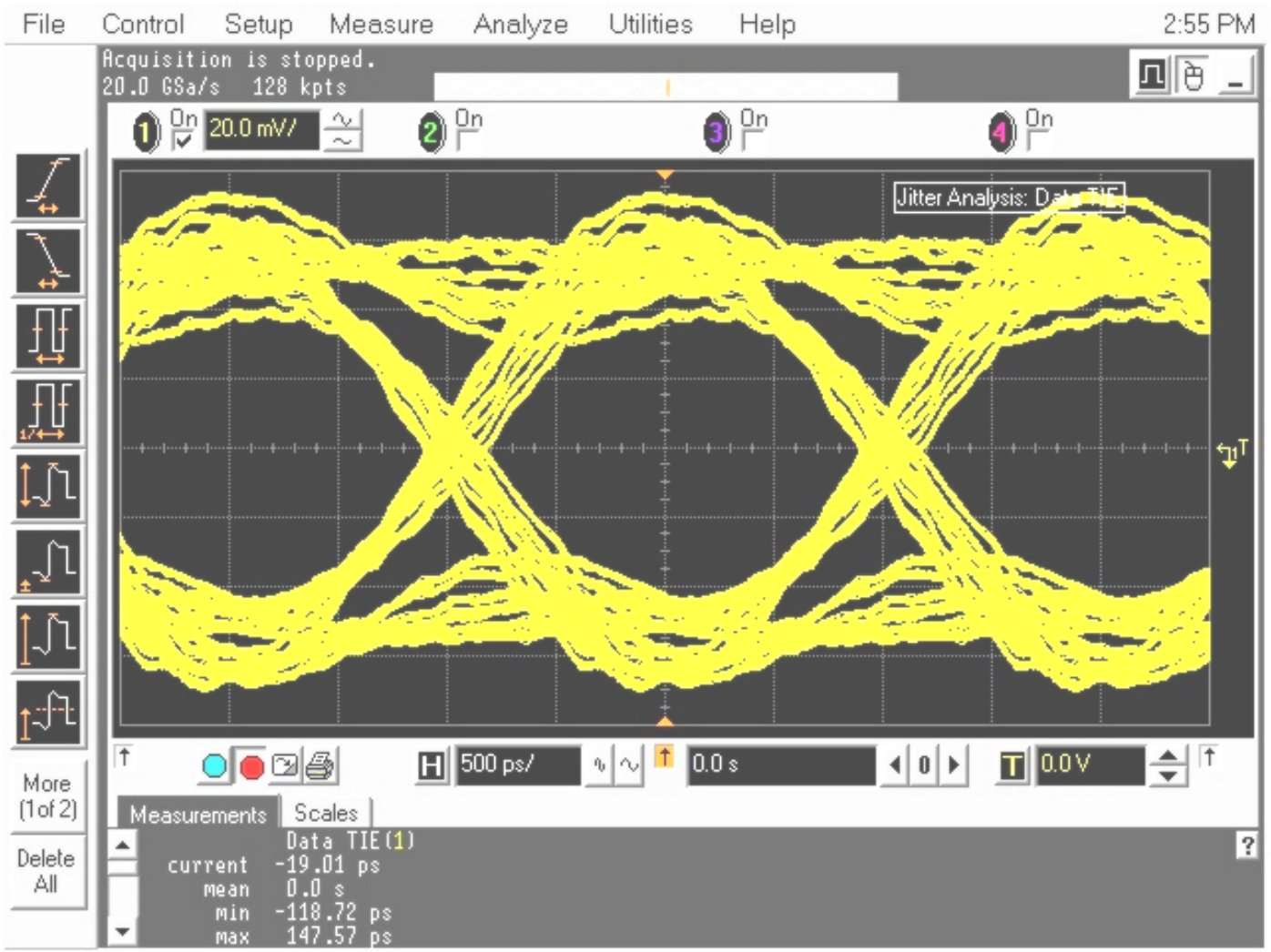
BW Limiting + Reflection



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Periodic Jitter

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Periodic Jitter

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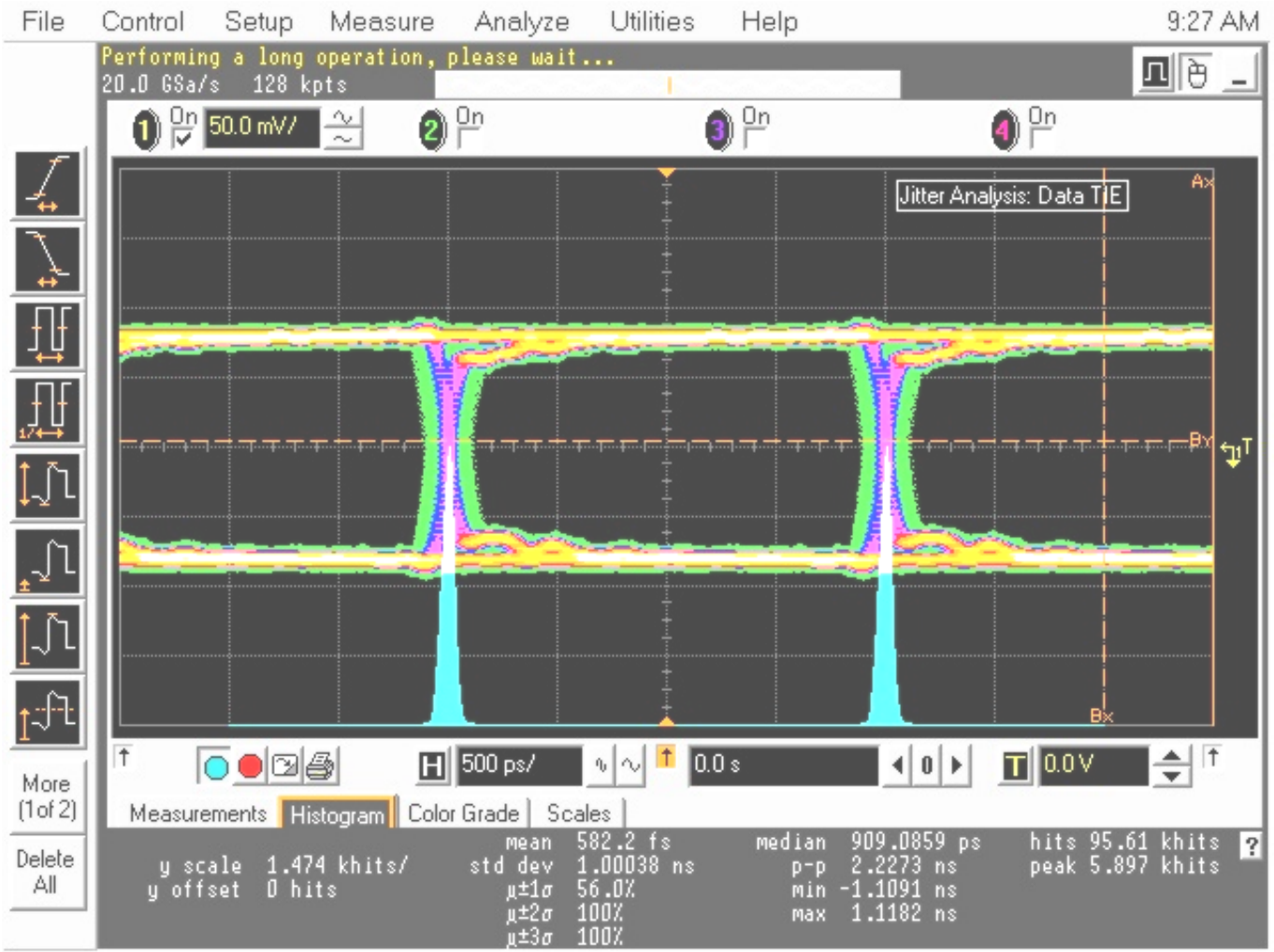
Random (Gaussian) Jitter



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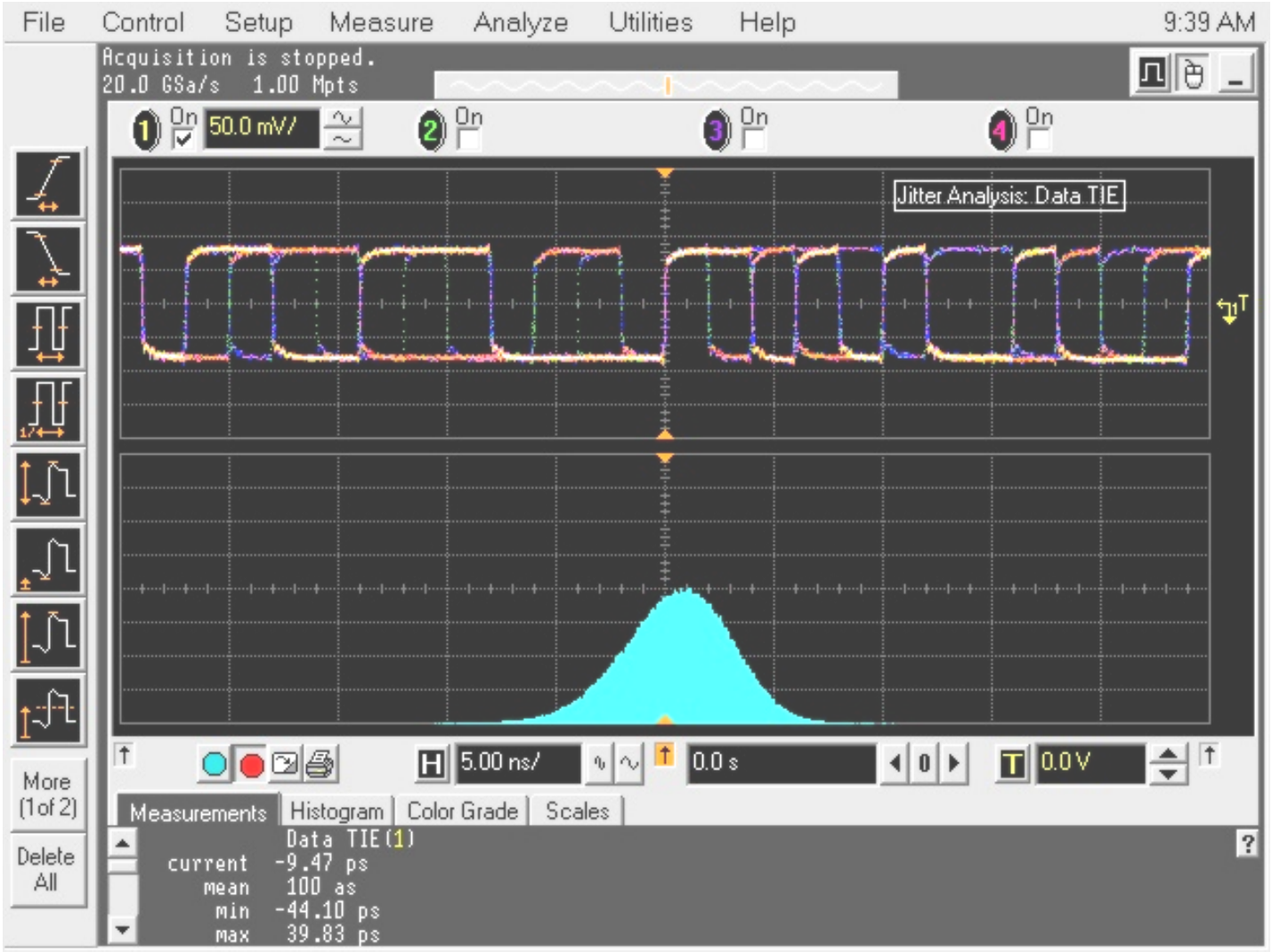
Random Jitter – TIE Histogram



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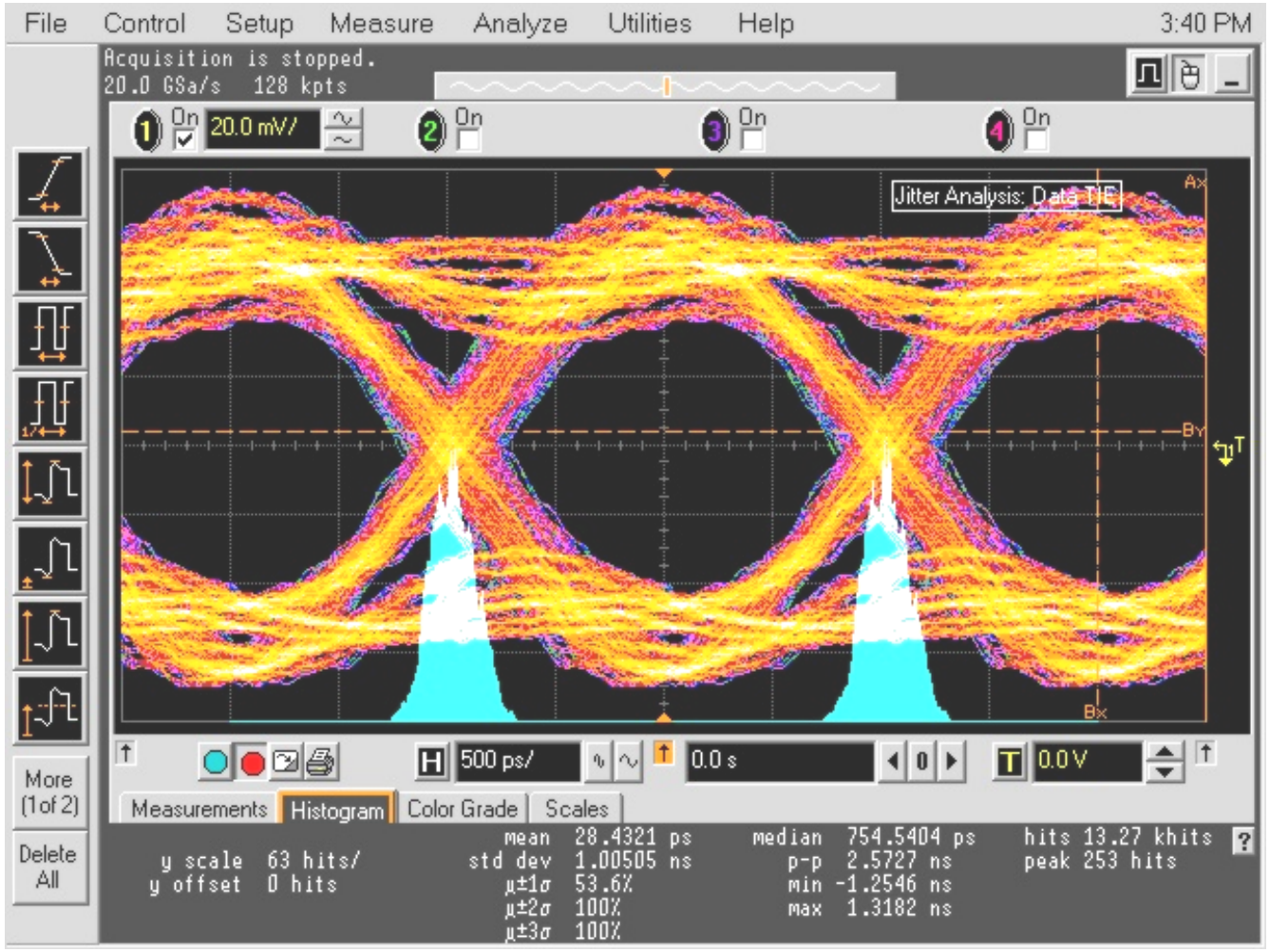
All Together Now



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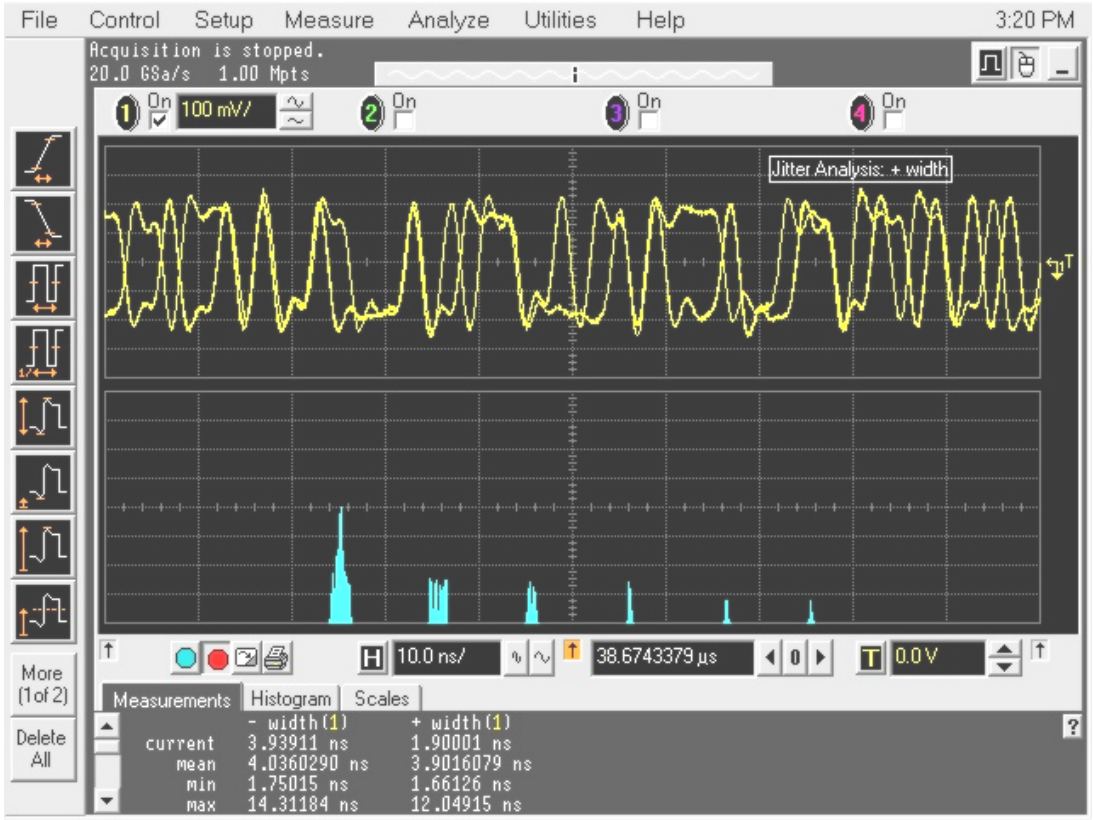
Duty Cycle Distortion - Causes

- Thresholding effects
- Non-symmetrical delays

Duty Cycle Distortion - Identifying

- Use jitter measurement
- Measure + and – widths
- Analyze histograms

Duty Cycle Distortion - Identifying



+ width histogram

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Duty Cycle Distortion - Identifying

Measure location of first peak – 1.89 ns

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Duty Cycle Distortion - Identifying

Note location of third peak = 5.96 ns

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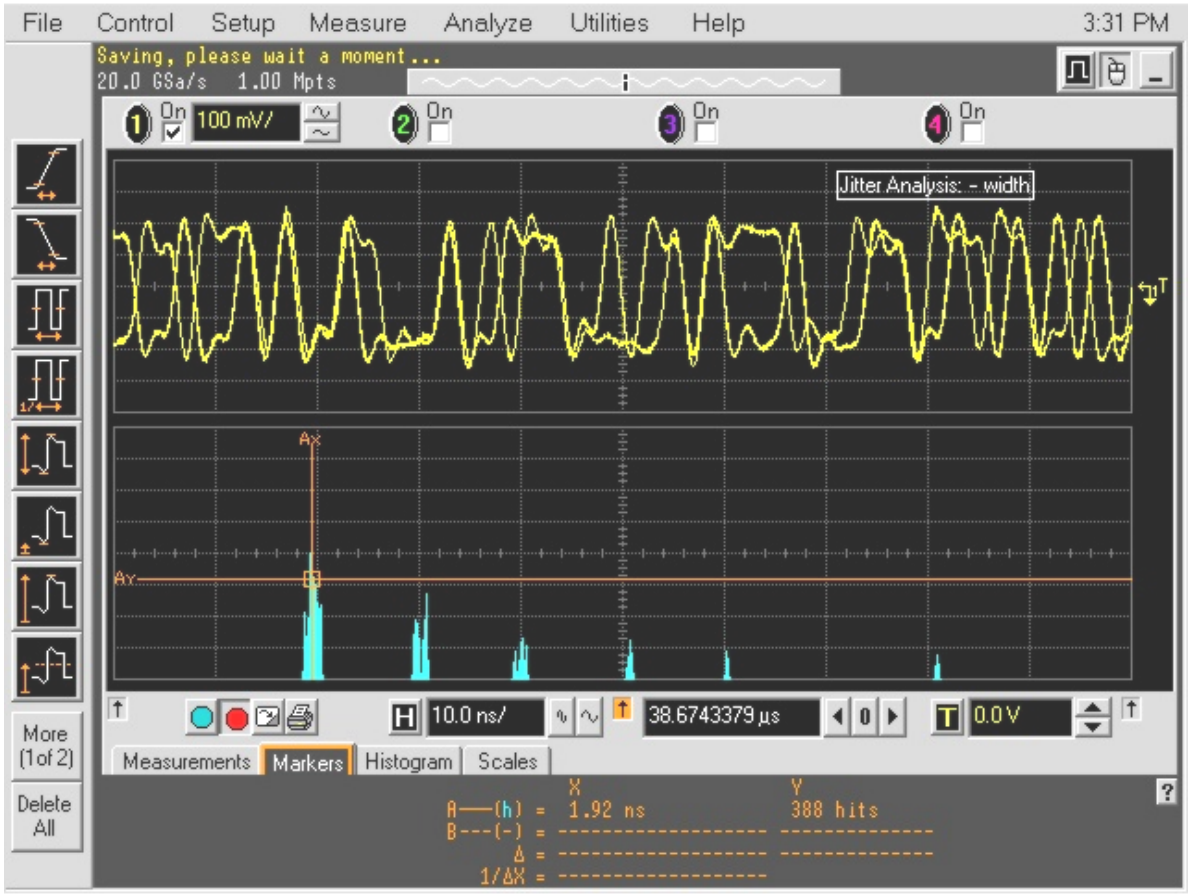
Duty Cycle Distortion - Identifying



Measure – width, put marker at the same spot, note shift of peak

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Duty Cycle Distortion - Identifying

Same for the third peak

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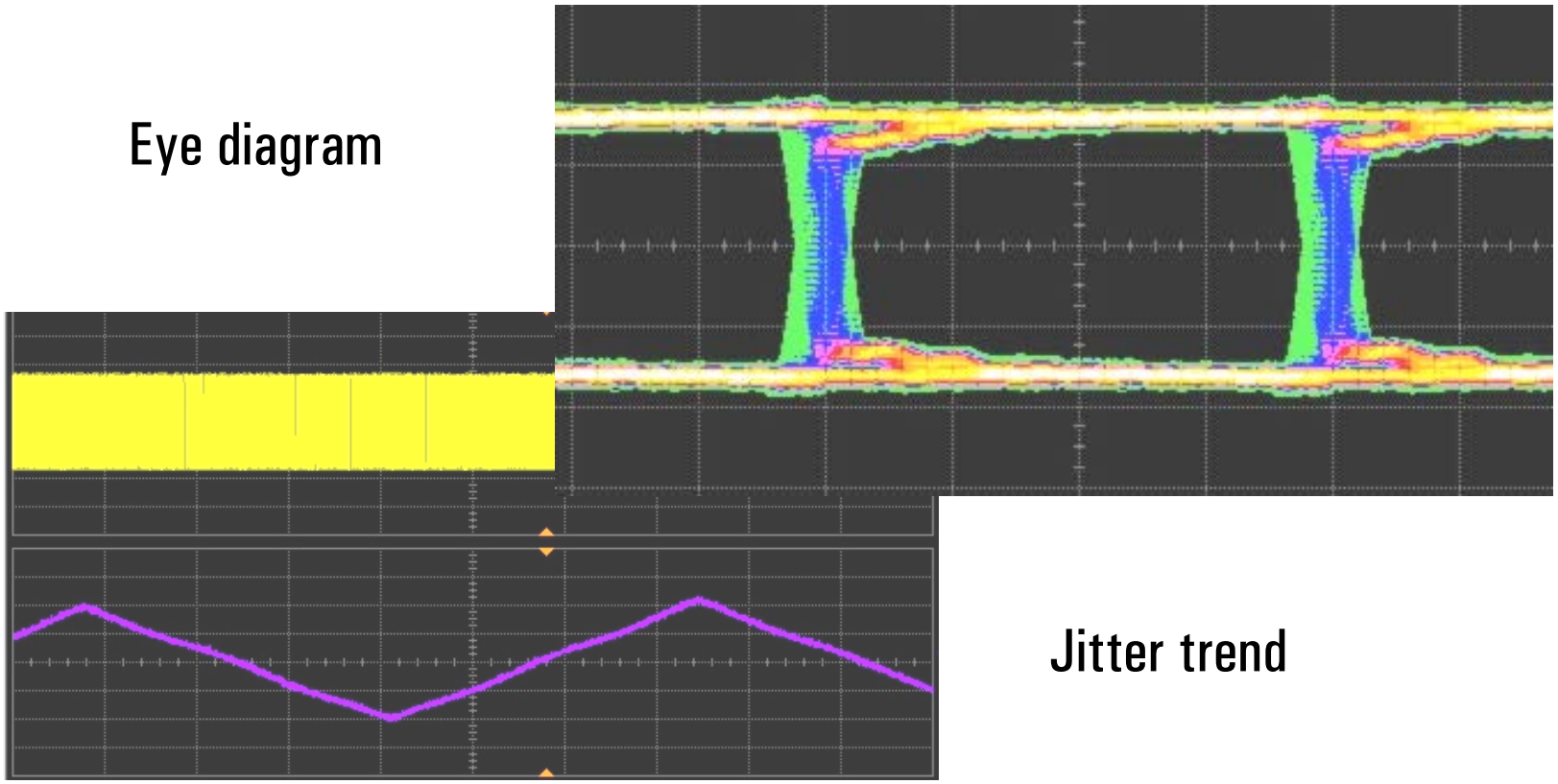
Spread-Spectrum Clocking

Eye diagram



Jitter trend

Spread spectrum clocking, without PLL

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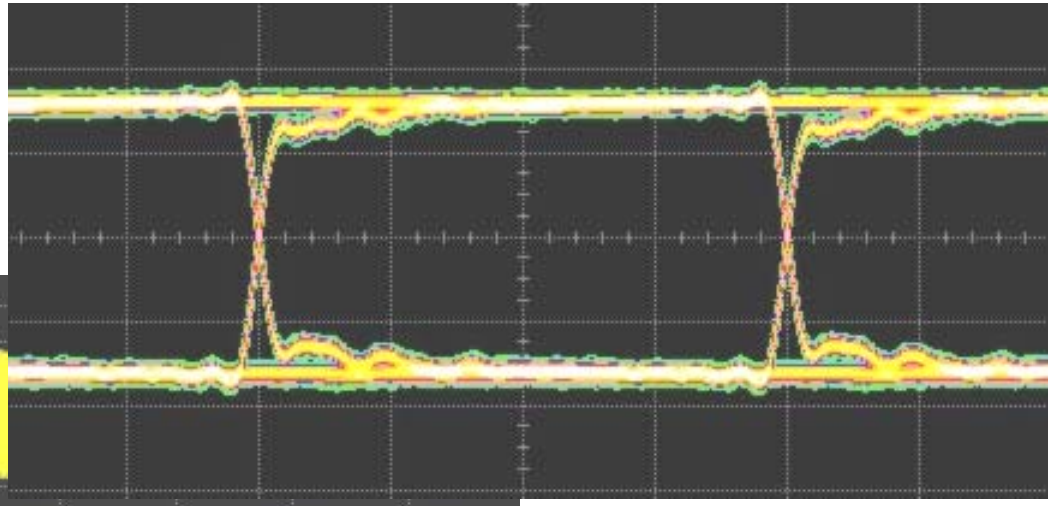
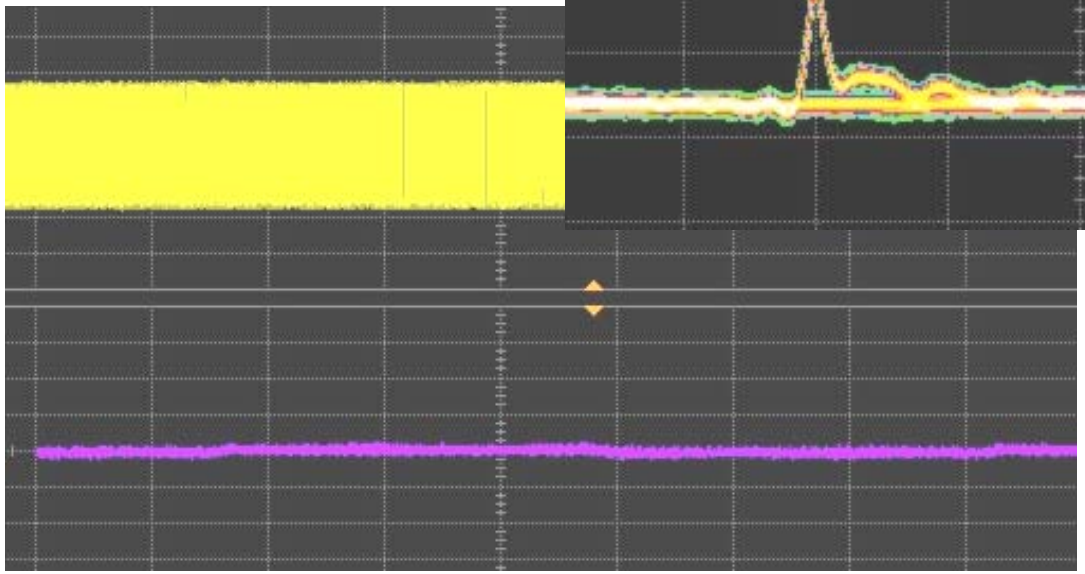
Spread-Spectrum Clocking

Eye diagram





Jitter trend

Spread spectrum clocking, with PLL

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Tools For Success

- Model development and verification
  - TDR
  - VNA, PLTS
- Verification, troubleshooting
  - Scope
  - Pulse/pattern generator
- Verification
  - BERT

Critical Parameters In a Scope

- Probing
- Time base stability
- Signal tracking accuracy at high speeds

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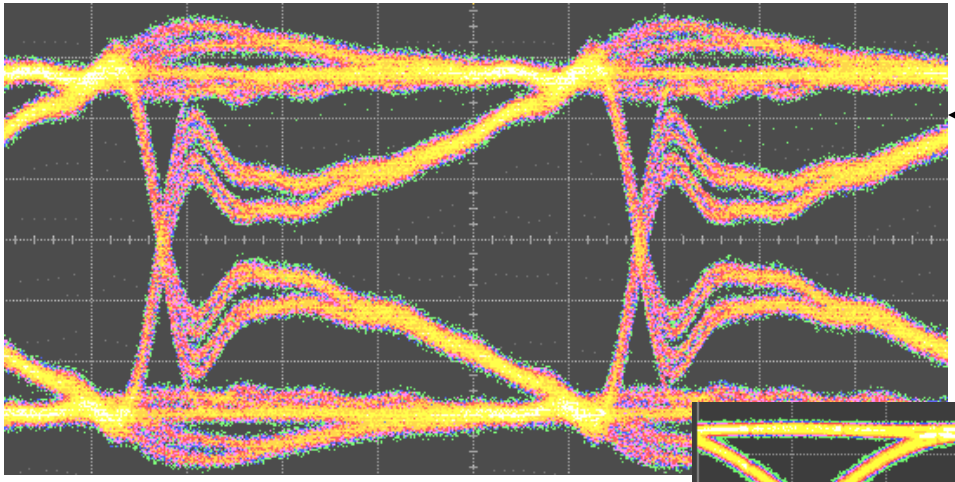
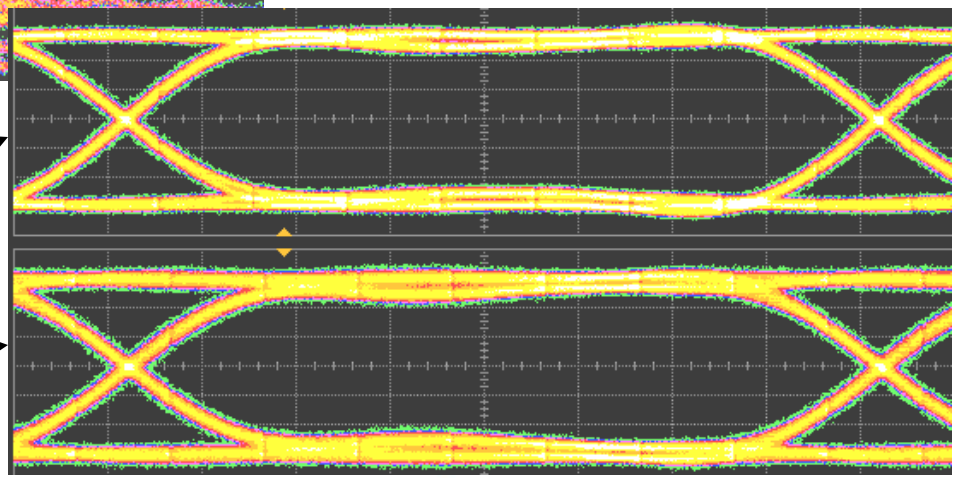
Probes Are Critical

Accurate measurements have to start at the probe tips



Impact of 1″
undamped wires

2.5 Gb/s eye



At probe input

Measured through probe

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Realtime Scope Measurement Tools

- Serial data analysis (e.g. Agilent E2688A)
- Jitter analysis
  - Agilent EZJIT
  - M1 Time Interval and Jitter Analysis

Summary

- Start with good models
- Understand statistical behavior
- Measure everything
- Know your tools

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Additional resources

www.agilent.com/find/si

http://www.agilent.com/find/jitter

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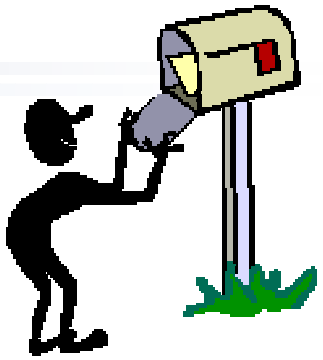
FREE Agilent Email Updates



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